WHAT IS CLAIMED IS:

1. A high speed adder in which provisional carriers composed of a pair of signals that indicate a case where carry is produced from a low order bit and a case where no carry is produced therefrom are generated in advance and an actual carrier is selected from the provisional carriers in accordance with selection information from the low order bit:

a carrier transfer path; and

a plurality of converters, each of which converts the provisional carriers into provisional sums composed of a pair of signals that indicate the case where the carry is produced from the low order bit and the case where no carry is produced therefrom, the converters being provided on a predetermined portion of the carrier transfer path.

2. An adder according to claim 1, wherein, when the adder is a 2^N(N is an integer of 3 or more)-bit adder, the carrier transfer path comprises (N+1) or less circuit stages,

wherein a first circuit stage receives two input data for each corresponding bit and an input carry signal from an outside, generates a bit sum of a least significant bit, outputs the bit sum to the outside, generates provisional carriers corresponding to each of bits other than the least significant bit, and outputs the generated provisional carriers to a following circuit stage,

wherein second to N-th circuit stages convert the provisional carriers corresponding to higher $(2^{(N-1)}-1)$ bits other than a most significant bit, of the provisional carriers into the provisional sums by at least one of the converters in course of transfer, and generate actual carriers from the provisional carriers corresponding to lower $(2^{(N-1)}-1)$ bits other

than the least significant bit, and

wherein a (N+1)-th circuit stage outputs data other than a bit sum of the least significant bit, of sum data of the two input data and an output carry signal to the outside.

3. An adder according to claim 2, wherein, when the input data is arranged in an order from the most significant bit to the least significant bit, at least one of the converters is located corresponding to a $(2^{(N-M-1)}+1)$-th bit to a $2^{(N-M)}$-th bit from the most significant bit of the input data in a (N-M+1)-th circuit stage which is specified by an integer M that satisfies $1 \leq M < N$.

4. An adder according to claim 2, wherein the first circuit stage comprises:

(2^N-1) conditional cells, each of which receives corresponding bits of the two input data to perform an exclusive OR operation, generates the provisional carriers composed of the pair of signals that indicate the case where the carry is produced from the low order bit and the case where no carry is produced therefrom, and outputs the generated provisional carriers, the conditional cells being provided corresponding to a most significant bit of 2^N bits to a bit higher than the least significant bit thereof by one; and

a full adder that receives the least significant bits of the two input data and the output carry signal and generates an exclusive OR signal and a carry signal.

5. An adder according to claim 4, wherein each of the conditional cells comprises:

a first gate that receives two input bits and performs an AND operation on the two input bits to output a first signal;

a second gate that receives the two input bits and performs an OR operation on the two input bits to output a second signal;

a third gate that receives the first signal outputted from the first gate and inverts the received first signal to output a third signal; and

a fourth gate that receives the second signal outputted from the second gate and the third signal outputted from the third gate and performs the AND operation on the second signal and the third signal to output a fourth signal,

wherein the first signal outputted from the first gate is given as a first carry signal which is the carry signal in the case where no carry is produced from the low order bit,

wherein the second signal outputted from the second gate is given as a second carry signal which is the carry signal in the case where the carry is produced from the low order bit, and

wherein the fourth signal outputted from the fourth gate is a result of the exclusive OR operation performed on the two input bits.

6. An adder according to claim 4, wherein, of the circuit stages, when the (N-M+1)-th circuit stage which is specified by the integer M that satisfies $1 \leq M < N$ is divided in a virtual form into 2^M sub-circuits corresponding to every $2^{(N-M)}$ bits of the input data,

the (N-M+1)-th circuit stage comprises:

$2^{(N-M-1)}$ multiplexers, each of which receives a pair of signals which are outputs of one of the conditional cell and

the carry selector which are provided for a corresponding bit in a preceding circuit stage; receives a signal outputted from one of the full adder and the multiplexer which are provided for a bit in a circuit stage preceding by one stage, and which corresponds to a $(2^{(N-M-1)}+1)$-th bit from a top in a first sub-arithmetic circuit; selects an actual carry signal in accordance with the received signal; and outputs the actual carry signal, the multiplexers being provided corresponding to higher $2^{(N-M-1)}$ bits of the first sub-arithmetic circuit which include an input from a bit corresponding to a $2^{(N-M)}$-th bit from the least significant bit in a high order direction;

$(2^{(N-1)} - 2^{(N-M-1)})$ carry selectors, each of which receives a pair of signals which are outputs of one of the conditional cell, the carry selector, and the converter, which are provided for the corresponding bit in the preceding circuit stage; receives a pair of selection signals which are outputs of one of the conditional cell and the carry selector which are provided for a bit in the circuit stage preceding by one stage, and which corresponds to the $(2^{(N-M-1)}+1)$-th bit from the top in a sub-circuit; selects a pair of signals indicating the provisional carriers or the provisional sums in the following circuit stage in accordance with the selection signals; and outputs the selected pair of signals, the carry selectors being provided corresponding to the higher $2^{(N-M-1)}$ bits in the sub-circuit which is included in a second sub-arithmetic circuit composed of a sub-circuit that receives a carry signal corresponding to the most significant bit or a third sub-arithmetic circuit composed of second to (2^M-1)-th sub-circuits from the second sub-arithmetic circuit in the low order direction; and

$2^{(N-M-1)}$ converters, each of which receives a pair of signals

which are outputs of one of the conditional cell and the carry selector which are provided for the corresponding bit in the preceding circuit stage and indicate the provisional carriers, and an exclusive OR signal outputted from the conditional cell corresponding to a bit higher by one bit in the first circuit stage; converts the received pair of signals into a pair of signals indicating the provisional sums; and outputs the pair of signals indicating the provisional sums, the converters being provided corresponding to lower $2^{(N-M-1)}$ bits in the second sub-arithmetic circuit.

7. An adder according to claim 6, wherein each of the conditional cells comprises:

a first gate that receives two input bits and performs an AND operation on the two input bits to output a first signal;

a second gate that receives the two input bits and performs an OR operation on the two input bits to output a second signal;

a third gate that receives the first signal outputted from the first gate and inverts the received first signal to output a third signal; and

a fourth gate that receives the second signal outputted from the second gate and the third signal outputted from the third gate and performs an AND operation on the second signal and the third signal to output a fourth signal,

wherein the first signal outputted from the first gate is given as a first carry signal which is the carry signal in the case where no carry is produced from the low order bit,

wherein the second signal outputted from the second gate is given as a second carry signal which is the carry signal in the case where the carry is produced from the low order bit,

and

wherein the fourth signal outputted from the fourth gate is a result of the exclusive OR operation performed on the two input bits.

8. An adder according to claim 6, wherein each of the converters comprises:

a first exclusive OR circuit that receives one of the pair of signals indicating the provisional carriers and the exclusive OR signal outputted from the conditional cell corresponding to the bit higher by one bit in the first circuit stage and outputs one of the pair of signals indicating the provisional sums; and

a second exclusive OR circuit that receives the other of the pair of signals indicating the provisional carriers and the exclusive OR signal, and outputs the other of the pair of signals indicating the provisional sums.

9. An adder according to claim 6, wherein each of the carry selectors comprises:

a first multiplexer that receives a pair of input signals indicating the provisional carriers, selects one of the pair of input signals in accordance with one of the pair of selection signals, and outputs the selected one as one of a pair of output signals; and

a second multiplexer that receives the pair of input signals, selects one of the pair of input signals in accordance with the other of the pair of selection signals, and outputs the selected one as the other of the pair of output signals.

10. An adder according to claim 6, wherein the (N+1)-th

circuit stage comprises:

a multiplexer that receives a pair of signals outputted from a highest order carry selector provided corresponding to the most significant bit of the input data in the N-th circuit stage, selects an output carry signal in accordance with the selection signal outputted the multiplexer corresponding to a $(2^{(N-1)}+1)$-th bit from the most significant bit of the input data in the low order direction in the N-th circuit stage, and outputs the output carry signal;

$(2^{(N-1)}-1)$ multiplexers, each of which receives the pair of signals outputted from one of the carry selector and the converter which are provided for a corresponding bit in the N-th circuit stage, selects a signal corresponding to an actual bit sum of a bit higher by one bit in accordance with the selection signal outputted from the multiplexer corresponding to the $(2^{(N-1)}+1)$-th bit from the most significant bit of the input data in the low order direction in the N-th circuit stage, and outputs the signal corresponding to an actual bit sum of a bit higher by one bit, the multiplexers being provided corresponding to a second bit to a $2^{(N-1)}$-th bit from the most significant bit of the input data in the low order direction; and

$2^{(N-1)}$ exclusive OR circuits, each of which receives the actual carry signal outputted from one of the full adder and the multiplexer which are provided for the corresponding bit in a preceding circuit stage and the exclusive OR signal outputted from the conditional cell corresponding to the bit higher by one bit in the first circuit stage, and outputs a signal corresponding to an actual bit sum of a bit higher by one bit, the exclusive OR circuits being provided corresponding to a $(2^{(N-1)}+1)$-th bit to a 2^{N}-th bit from the most significant bit

of the input data in the low order direction.

11. An adder according to claim 10, wherein each of the conditional cells comprises:

a first gate that receives two input bits and performs an AND operation on the two input bits to output a first signal;

a second gate that receives the two input bits and performs an OR operation on the two input bits to output a second signal;

a third gate that receives the first signal outputted from the first gate and inverts the received first signal to output a third signal; and

a fourth gate that receives the second signal outputted from the second gate and the third signal outputted from the third gate and performs the AND operation on the second signal and the third signal to output a fourth signal,

wherein the first signal outputted from the first gate is given as a first carry signal which is the carry signal in the case where no carry is produced from the low order bit,

wherein the second signal outputted from the second gate is given as a second carry signal which is the carry signal in the case where the carry is produced from the low order bit, and

wherein the fourth signal outputted from the fourth gate is a result of the exclusive OR operation on the two input bits.

12. An adder according to claim 10, wherein each of the converters comprises:

a first exclusive OR circuit that receives one of the pair of signals indicating the provisional carriers and the exclusive OR signal outputted from the conditional cell corresponding to

the bit higher by one bit in the first circuit stage, and outputs one of the pair of signals indicating the provisional sums; and

a second exclusive OR circuit that receives the other of the pair of signals indicating the provisional carriers and the exclusive OR signal, and outputs the other of the pair of signals indicating the provisional sums.

13. An adder according to claim 10, wherein each of the carry selectors comprises:

a first multiplexer that receives a pair of input signals indicating the provisional carriers, selects one of the pair of input signals in accordance with one of the pair of selection signals, and outputs the selected one as one of a pair of output signals; and

a second multiplexer that receives the pair of input signals, selects one of the pair of input signals in accordance with the other of the pair of selection signals, and outputs the selected one as the other of the pair of output signals.